IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION OF ACCURACY OF TRANSLATION IN LIEU OF SWON TRANSLATION (37 C.F.R. § 1.68)

The undersigned translator, Masao Mitsuyoshi, serving in a firm of Suzuki International Patent Office located in c/o Chanokiya Bldg. 5F, No. 3-1, Nihonbashi-Honcho 2-chome, Chuo-ku, Tokyo 103-0023, Japan, hereby certifies and declares that:

(1) I am fully conversant with both the Japanese language and the English language;

(2) I have translated the Japanese-language specification of the Japanese patent application, entitled "SEMICONDUCTOR DEVICE AND METHOD AND APPARATUS FOR MANUFACTURING THE SAME" filed on June 20, 2000 in the Japanese Patent Office under the Filing No. 2000-185275 (185275/2000), into English, the Japanese-language specification being filed as a certified priority document in the United States Patent and Trademark Office together with the United States patent application entitled "SEMICONDUCTOR DEVICE AND METHOD AND APPARATUS FOR MANUFACTURING THE SAME" and filed on June 19, 2001 under Serial No. 09/883,370. A copy of the English translation is attached hereto; and

(3) The attached English translation is, to the best of my knowledge, and belief, an accurate and literal translation from the Japanese language into the English language.

The undersigned, Masao Mitsuyoshi, hereby declares further that all statements herein of my own knowledge are true; and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the matter with which this translation is used.

On this 11th day of April, 2003

Masao Mitsuyoshi

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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF INVENTION] SEMICONDUCTOR DEVICE AND METHOD AND APPARATUS FOR MANUFACTURING THE SAME

[SCOPE OF CLAIM FOR PATENT]

[Claim 1] In a semiconductor device in which an interlevel insulating film formed between a Cu interconnection, formed by damascene, and an upper metal interconnection layer formed on the Cu interconnection has a multilayered structure made up of a Cu diffusion preventive insulating layer and another insulating film, and when a connection hole for connecting the Cu interconnection and the upper metal interconnection layer to each other is to be formed in the interlevel insulating film by dray etching, the connection hole is formed to reach the Cu diffusion preventive insulating layer, a photoresist is removed, and thereafter the Cu diffusion preventive insulating film is removed, characterized in that said Cu diffusion preventive insulating layer has a multilayered structure made of not less than two layers.

[Claim 2] A semiconductor device as set forth in claim 1, wherein said Cu diffusion preventive insulating layer has a multilayered structure made up of a first Cu diffusion preventive insulating film formed by CVD at a low temperature of less than 350°C and a second Cu diffusion preventive insulating film formed by CVD at a high temperature of not less than 350°C and not more than 450°C.

[Claim 3] A semiconductor device as set forth in claim

1 or 2, wherein an oxide layer on a Cu surface, which is formed between said Cu diffusion preventive insulating layer and said Cu interconnection, is reduced in order to improve adhesion properties of said Cu diffusion preventive insulating layer.

[Claim 4] A semiconductor device as set forth in either one of claims 1, 2 and 3, wherein said first Cu diffusion preventive insulating film is an insulating film not containing O.

[Claim 5] A semiconductor device as set forth in claim 4, wherein said first Cu diffusion preventive insulating film not containing O is one film selected from the group consisting of an SiN film, SiC film, SiCN film, and organic film.

[Claim 6] A semiconductor device as set forth in claim 2, wherein a dry etching selectivity of said second Cu diffusion preventive insulating film to said interlevel insulating film formed on said second Cu diffusion preventive insulating film is not less than 1 : 10.

[Claim 7] In a method of manufacturing a semiconductor device in which an interlevel insulating film formed between a Cu interconnection formed by damascene and an upper metal interconnection layer formed on said Cu interconnection has a multilayered structure made of a Cu diffusion preventive insulating layer and another insulating film, characterized in that said Cu diffusion preventive insulating layer has a multilayered structure made of not less than two layers.

[Claim 8] A method of manufacturing a semiconductor device as set forth in claim 7, wherein said Cu diffusion preventive layer is formed by forming a first Cu diffusion preventive insulating film by CVD at a low temperature of less than 350°C, and forming a second Cu diffusion preventive insulating film by CVD at a high temperature of not less than 350°C and not more than 450°C.

[Claim 9] An apparatus for manufacturing a semiconductor device in which a Cu diffusion preventive insulating layer is formed on a Cu interconnection, wherein said apparatus has a function of forming a first Cu diffusion preventive insulating layer by CVD at a low temperature of less than 350°C, and forming a second Cu diffusion preventive insulating layer by CVD at a high temperature of not less than 350°C and not more than 450°C.

[DETAILED DESCRIPTION OF INVENTION]

[0001]

[Technical field to which the invention belongs]

The present invention relates to a semiconductor device and a method and an apparatus for manufacturing the same and, more particularly, to a Cu diffusion preventive insulating layer in an interlevel insulating film formed between a Cu interconnection and a metal interconnection on it.

[0002]

[Prior art]

In the IC manufacturing field, as the operation speed and integration degree of devices increase, the device design

rule decreases. As the device feature size decreases, the interconnection size and the gap between interconnections also decrease, so the interconnection resistance and the parasitic capacitance between interconnections tend to increase.

[0003]

When the interconnection resistance or parasitic capacitance between interconnections increases, the RC time constant increases, and the signal propagation speed decrease to pose a problem in increasing the operation speed of the device. The parasitic capacitance between interconnections increases in proportion to the area of the interconnections and the relative dielectric constant of an insulating film between the interconnections, and in inverse proportion to the gap between the interconnections. To decrease the parasitic capacitance without changing the device design, it is effective to decrease the relative dielectric constant of the insulating film.

[0004]

In recent years, various types of interlevel insulating films with low dielectric constants, e.g., an SiOF film with a lower relative dielectric constant than that of a conventional SiO_2 film, has been studied in order to decrease the capacitance between interconnections. To decrease the interconnection resistance, a technique which uses as an interconnection material Cu with a lower resistivity than that of Al conventionally used widely as the interconnection

material, and products as a result of this technique have become popular.

[0005]

When Cu is used as the interconnection material, since it is difficult to micropattern Cu by dry etching, a damascene interconnection structure as shown in Fig. 1 is usually used widely. A damascene interconnection is formed in the following manner. A trench 20 is formed in an interlevel film 6, and is filled with a barrier metal 10 and Cu. Excessive Cu and barrier metal on the insulating film are removed by CMP, thus forming a Cu interconnection 12.

[0006]

If an interlevel insulating film is to be formed after formation of the damascene interconnection, as Cu easily reacts with SiO_2 and diffuses, an SiN film 52 is usually formed as a diffusion preventive insulating film on Cu to a thickness of about 50 nm to 100 nm in accordance with parallel-plate plasma CVD by using SiH_4, NH_3, and N_2, and after that an insulating film 20 of SiO_2 or the like is formed.

[0007]

In this case, SiN not only prevents Cu diffusion but also prevents the Cu surface from being exposed to the SiO_2 etching or O_2 resist ashing atmosphere when, e.g., a via hole is to be formed on the Cu damascene interconnection, so it also serves as an etching stop layer for SiO_2. In this manner, the SiN film 52 formed on the Cu surface must prevent

Cu diffusion and serve as an etching stop layer.

[0008]

[Problems to be solved by the present invention]

1. Usually, when a SiN film is to be formed on a Cu surface, as the film formation temperature is about 400 degrees of Celsius thermometer, as the substrate temperature increases, aggregation of Cu tends to occur, and the morphology of the Cu surface degrades. Hence, a diffusion preventive insulating layer in which aggregation of Cu is suppressed is necessary.

[0009]

2. One of methods of suppressing aggregation of Cu is to decrease the film formation temperature. When the film formation temperature is decreased, SiN forms a low-density insulating film. If the insulating film has a low density, the etching selectivity with respect to SiO_2 decreases, and the SiN film cannot serve as an etching stop layer. For this reason, a dense film for maintaining the etching selectivity with respect to the insulating film is necessary as a diffusion preventive layer.

[0010]

In a semiconductor device and a method and apparatus for manufacturing the same, it is an object of the present invention to provide a semiconductor device in which an interlevel insulating film enabling to suppress aggregation of Cu and having a sufficiently high etching selectivity with respect to an insulating film is formed, and a method and

apparatus for manufacturing the same.

[0011]

[Means for solving the problem]

In a semiconductor device in which an interlevel insulating film formed between a Cu interconnection, formed by damascene, and an upper metal interconnection layer formed on the Cu interconnection has a multilayered structure made up of a Cu diffusion preventive insulating layer and another insulating film, and when a connection hole for connecting the Cu interconnection and the upper metal interconnection layer to each other is to be formed in the interlevel insulating film by dray etching, the connection hole is formed to reach the Cu diffusion preventive insulating layer, a photoresist is removed, and thereafter the Cu diffusion preventive insulating film is removed, a semiconductor device of the present invention has such a Cu diffusion preventive insulating layer as having a multilayered structure made of not less than two layers.

[0012]

Further, the Cu diffusion preventive insulating layer has a multilayered structure in which a first Cu diffusion preventive insulating film is formed by CVD at a temperature of less than 350°C and in which a second Cu diffusion preventive insulating film is formed by CVD at a high temperature of not less than 350°C and not more than 450°C.

[0013]

In order to improve adhesion properties of said Cu

diffusion preventive insulating layer, a pre-process is applied between the Cu diffusion preventive insulating layer and the Cu interconnection. The pre-process is, for example, such a process as reducing an oxide layer on a surface of Cu, or the like. The first Cu diffusion preventive insulating film is an insulating film not containing O, and the first Cu diffusion preventive insulating film not containing O is one film selected from the group consisting of an SiN film, SiC film, SiCN film, and organic film.

[0014]

A dry etching selectivity of the second Cu diffusion preventive insulating film to the interlevel insulating film formed on the second Cu diffusion preventive insulating film is not less than 1 : 10.

[0015]

In a semiconductor device in which an interlevel insulating film formed between a Cu interconnection, formed by damascene, and an upper metal interconnection layer formed on the Cu interconnection has a multilayered structure made up of a Cu diffusion preventive insulating layer and another insulating film, and when a connection hole for connecting the Cu interconnection and the upper metal interconnection layer to each other is to be formed in the interlevel insulating film by dray etching, the connection hole is formed to reach the Cu diffusion preventive insulating layer, a photoresist is removed, and thereafter the Cu diffusion preventive insulating film is removed, a semiconductor device

manufacturing method of the present invention makes the Cu diffusion preventive insulating layer into a multilayered structure made of not less than two layers.

[0016]

According to the semiconductor device manufacturing method, the Cu diffusion preventive layer is formed by forming a first Cu diffusion preventive insulating film by CVD at a low temperature of less than 350°C, and forming a second Cu diffusion preventive insulating film by CVD at a high temperature of not less than 350°C and not more than 450°C.

[0017]

In an apparatus for manufacturing a semi-conductor device in which a Cu diffusion preventive insulating layer is formed on a Cu interconnection, the apparatus for manufacturing a semi-conductor device is adapted to have functions of forming a first Cu diffusion preventive insulating layer by CVD at a low temperature of less than 350°C, and forming a second Cu diffusion preventive insulating layer by CVD at a high temperature of not less than 350°C and not more than 450°C.

[0018]

In this manner, a Cu diffusion preventive insulating layer with a multilayered structure can be formed, in which a first insulating film SiN is so formed on the Cu interconnection at a low temperature of less than 350°C as to suppress aggregation of Cu and in which a second insulating

film SiN is so formed at a high temperature of not less than 350°C and not more than 450°C as to highly improve functions as an etch stop layer.

[0019]

[Exemplified embodiment of the invention]

Hereinafter, an exemplified embodiment of a semiconductor device of the present invention will be described.

[0020]

A process of manufacturing a semiconductor device is shown Fig. 1, Fig. 2, Fig. 3. First of al, as shown in Fig. 1(a), an SiO_2 insulating film 6 is formed on a silicon substrate 4 with a device element to a thickness of 500 nm by plasma CVD. Subsequently, a photoresist 8 is applied to the SiO_2 insulating film 6, and a trench interconnection pattern is formed by photolithography. Subsequently, as shown in Fig. (1b), after the insulating film 6 is etched by dry etching to form a trench, the photoresist 8 is removed by O_2 dry ashing and wet etching. And then, Ta 10 is formed as a barrier metal to a thickness of 50 nm, and a Cu film is formed by sputtering to a thickness of 100 nm as a seed layer for Cu plating on the entire surface of the silicon substrate 4.

[0021]

Next, the trench is filled with Cu 14 by electrolytic plating, and Cu is annealed at 400°C. Then, as shown in Fig. 1(d), the Cu 14 and barrier metal 10 on the insulating film 6 are removed by CMP, thus forming the Cu inter-

connection 12.

[0022]

Next, as shown in Fig. 2(a), by using a single-wafer type parallel-plate CVD apparatus, a diffusion preventive insulating layer SiN as a first insulating film 16 is formed to a thickness of 20 nm by low-temperature film formation with a film formation temperature of 300°C, an SiH_4 flow rate of 50 sccm, an NH_3 flow rate of 30 sccm, an N_2 flow rate of 2,000 sccm, a film formation pressure of 4 Torr, and an RF power of 400 W. Subsequently, by using another film formation chamber, a diffusion preventive insulating layer SiN as a second insulating film 18 is formed to a thickness of 30 nm by high-temperature film formation with a film formation temperature of 400°C, an SiH_4 flow rate of 50 sccm, an NH_3 flow rate of 30 sccm, an N_2 flow rate of 2,000 sccm, a film formation pressure of 4 Torr, and an RF power of 400 W. After that, as shown in Fig. 2(b), a 500-nm thick SiO_2 film is formed by plasma CVD and an insulating film 20 as another insulating film is formed on the Cu interconnection 14. The first insulating film 16, the second insulating film 18 and the insulating film 20 make up the interlevel insulating film.

[0023]

Next, how to form a via hole in the interlevel insulating film comprised of the insulating film 20 and the like will be described. As shown in Fig. 2(c), a pattern for forming a via hole is formed with a photoresist 22 by photolithography, and the SiO_2 film as the insulating film 20

is etched by dry etching using C_4F_8, Ar, and O_2 (see Fig. 2H). In this case, the etching conditions are determined such that the etching selectivity of the Cu diffusion preventive insulating film of the insulating film 20 to that of the second insulating film 18 is 10 or more, so the Cu diffusion preventive insulating film of the second insulating film 18 serves as the etching stop layer when etching the insulating film 20.

[0024]

Next, as shown in Fig. 3(a), the photoresist 22 is removed by O_2 ashing and resist peeling technique using a wet etchant. At this time, oxidation and etching of the first and second insulating films 16 and 18, which occur when the surface of a Cu interconnection 12 is exposed to an O_2 plasma and the like, are prevented.

[0025]

Then, as shown in Fig. 3(b), the Cu diffusion preventive insulating layer comprised of the first insulating layer 16 and the second insulating layer 18 is etched by dry etching using C_4F_8 and Ar, to form a via hole 30. Subsequently, as shown in Fig. 3(c), a TiN film 11 is formed to a thickness of 50 nm, and thereafter a W (tungsten) film 32 is formed to a thickness of 700 nm so as to fill the via hole 30 with W 32, and the excessive W film 32 and TiN film 11 on the interlevel insulating film 20 are removed by CMP, thus forming a via contact with respect to the Cu interconnection 14.

[0026]

In the above case, SiN is used to form the diffusion preventive insulating layer comprised of the first and second insulating films 16 and 18. Alternatively, an insulating film such as a SiC, SiCN, or organic film which does not react with Cu and thus serves to prevent diffusion of Cu may be employed. To form the insulating film 20, SiO_2 is used. Alternatively, an insulating layer, e.g., a porous silica, organic, HSQ, or MSQ film, with a lower relative dielectric constant than that of SiO_2 may be used.

[0027]

(Another Exemplified Embodiment)

In another exemplified embodiment, a Cu interconnection 12 is formed in accordance with the same method as that of the aforementioned embodiment. Subsequently, in order to reduce the oxide layer on the Cu surface, a plasma pre-process is carried out by using a parallel-plate CVD apparatus under the condition of a process temperature of 300°C, an N_2 flow rate of 500 sccm, an NH_3 flow rate of 500 sccm, a pressure of 4 Torr, and an RF power of 200 W. After that, a diffusion preventive insulating layer SiN as a first insulating film 16 is formed to a thickness of 20 nm with the same conditions as those of the first embodiment.

[0028]

Subsequently, by using another CVD apparatus, a diffusion preventive insulating layer SiC as a second insulating film 18 is formed to a thickness of 30 nm under

the condition of a film formation temperature of 400°C. Further, an SiO_2 layer as an insulating film 20 is formed to a thickness of 500 nm by the parallel-plate plasma CVD apparatus, thereby forming the insulating film 20 on the Cu interconnection 14.

[0029]

In another exemplified embodiment, the pre-process for reducing the Cu oxide layer is carried out at 300°C. This is sufficient as far as aggregation of Cu is suppressed at less than 350°C. Although a plasma pre-process is carried out here, annealing in a reducing gas atmosphere of NH_3 or H_2 may be carried out instead. Although N_2 and NH_3 are used as gases for the pre-process, a single-gas atmosphere of H_2 or NH_3, or a gas mixture atmosphere of N_2, H_2 and NH_3 may be used instead. The gas type is not particularly specified as far as it can reduce the oxide layer on the Cu surface. A process chamber for performing the plasma pre-process may be provided independently of the SiN film formation chamber.

[0030]

In another exemplified embodiment, SiN is used to form the Cu diffusion preventive insulating layer of the first insulating film 16, and SiC is used to form the Cu diffusion preventive insulating layer of the second insulating film 18. Alternatively, an SiCN, organic, or SiON film may be used as each insulating film. The diffusion preventive layers formed of the first insulating film 16 and the second insulating film 18 need not have the same film composition, and are not

particularly specified as far as they have an etching selectivity of a predetermined value or more with respect to the insulating film 20. In addition, in another exemplified embodiment, a Cu diffusion preventive insulating layer of a double-layered structure is formed. Alternatively, a multilayered structure of more than double-layers may be employed. The present invention is not particularly specified in this respect as well.

[0031]

Further, as the manufacturing apparatus, the CVD apparatus is so constructed as to form the first insulating film 16 at a temperature of about 300°C and form the second insulating film 18 at a temperature of about 400°C. Except for that, the arrangement of the manufacturing apparatus can be the same as that of a conventional apparatus.

[0032]

[Effect of the Invention]

A first effect of the present invention is that it can suppress aggregation of Cu in the Cu interconnection. The reason aggregation of Cu is suppressed is because the first insulating film is formed at a low temperature of less than 350°C.

[0033]

A second effect of the present invention is that it can improve the etching selectivity of the insulating film to the Cu diffusion preventive insulating layer (e.g., SiO_2 and SiN). The reason is it is so because, since a Cu diffusion

preventive insulating layer has a multilayered structure made of not less than two layers, and further the second Cu diffusion preventive insulating film is formed at a high temperature of not less than 350°C and not more than 450°C, such a Cu diffusion preventive insulating layer as being denser and having a better film quality than a Cu diffusion preventive insulating layer formed at a temperature of less than 350°C can be formed.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

(a), (b), (c), (d) are views showing a process of manufacturing a semiconductor device according to the present invention in the order of its steps.

[Fig. 2]

(a), (b), (c), (d) are views showing a process of manufacturing a semiconductor device according to the present invention in the order of its steps.

[Fig. 3]

(a), (b), (c) are views showing a process of manufacturing a semiconductor device according to the present invention in the order of its steps.

[Fig. 4]

This is an explanatory view showing the prior art.

[DESCRIPTION OF REFERENCE NUMERAL]

4 Silicon Substrate

6 Insulating Film

8, 22 Photoresist

10, 11 Ta

12 Cu Interconnection

14 Cu

16 First Insulating Film

18 Second Insulating Film

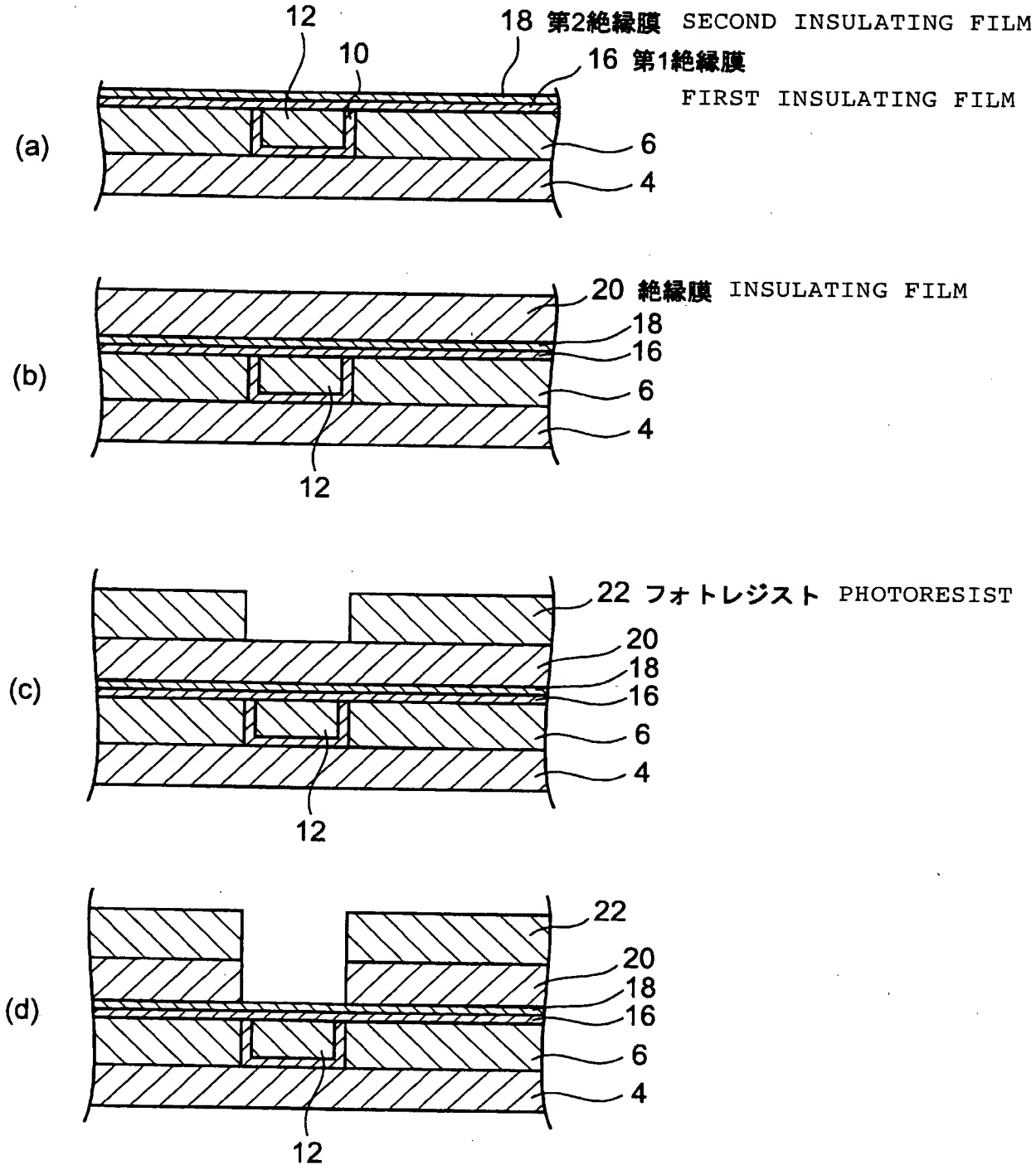
20 Insulating Film

30 Via Hole

32 W

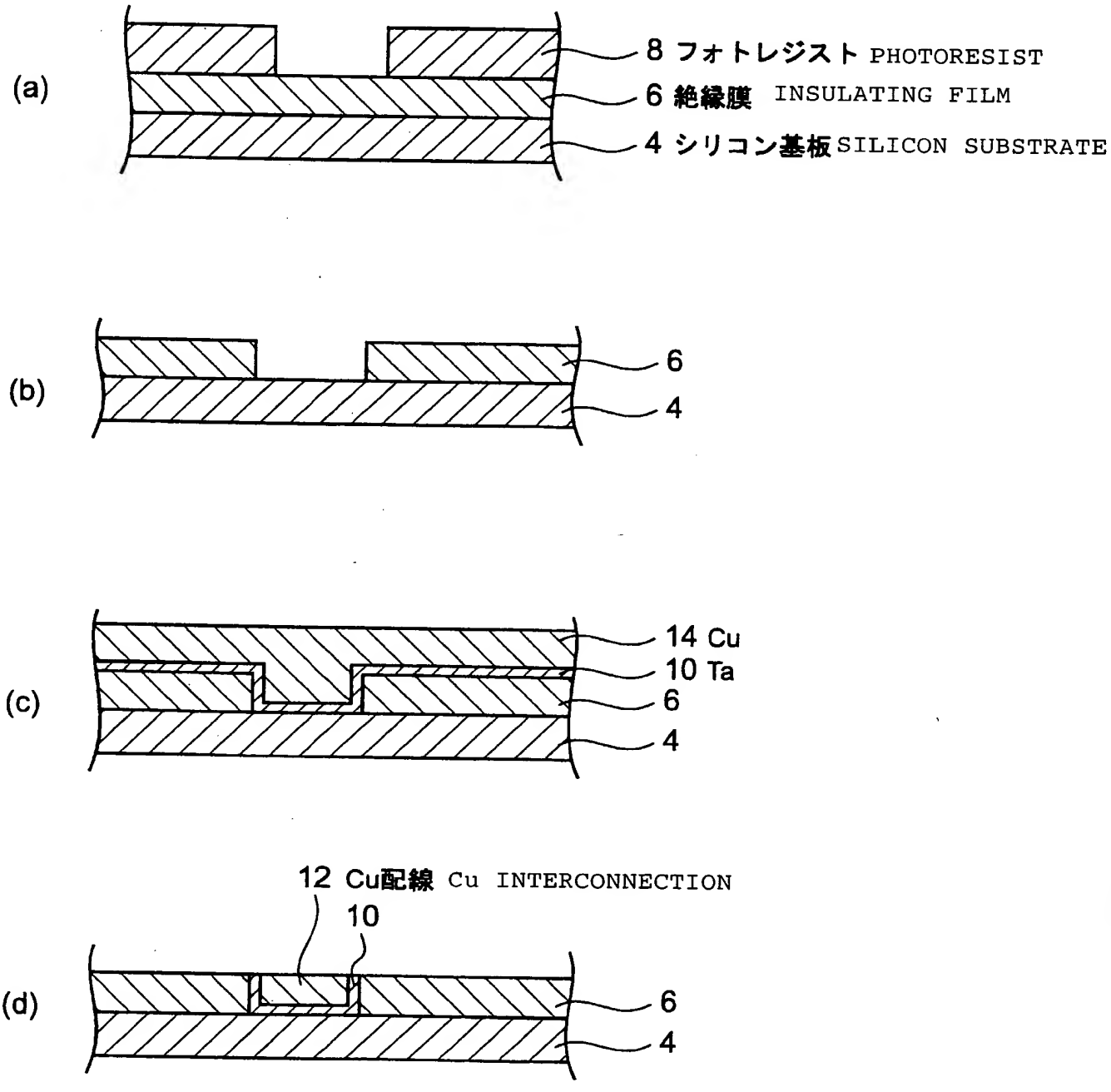
52 SiN Film

【図２】 Fig. 2

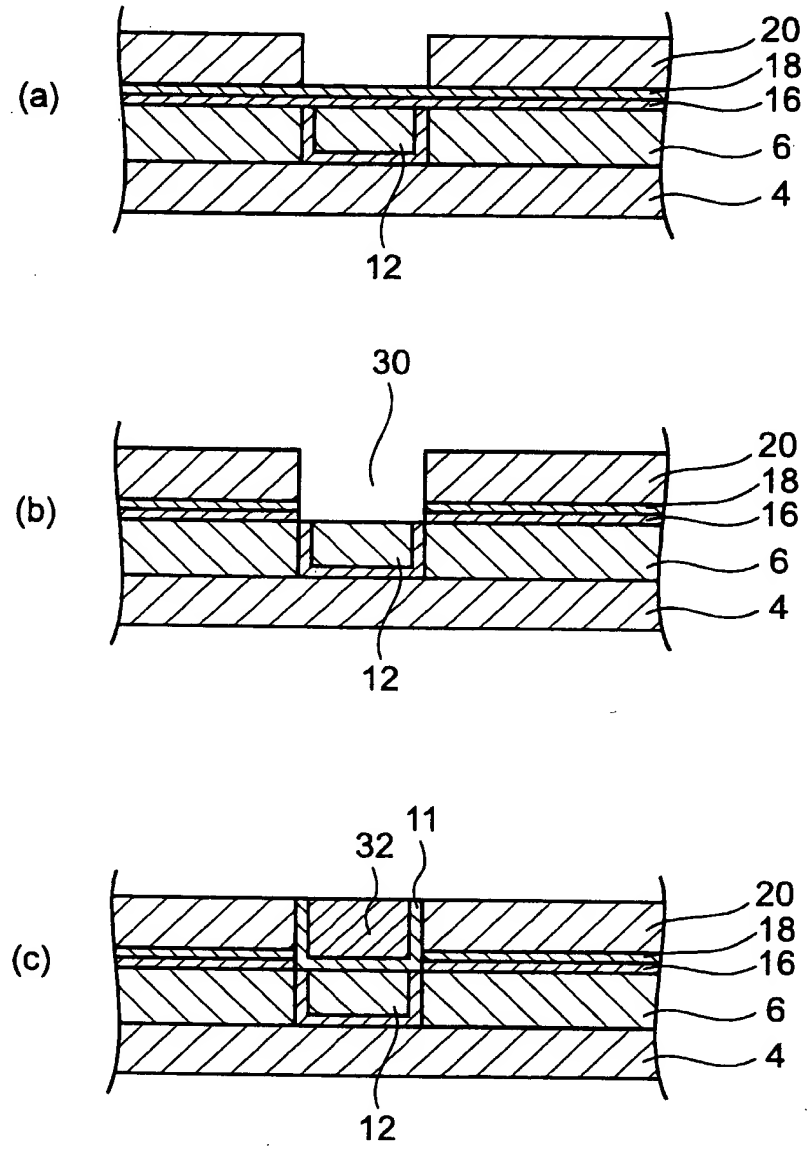


NAME OF DOCUMENT DRAWINGS
【書類名】 図面

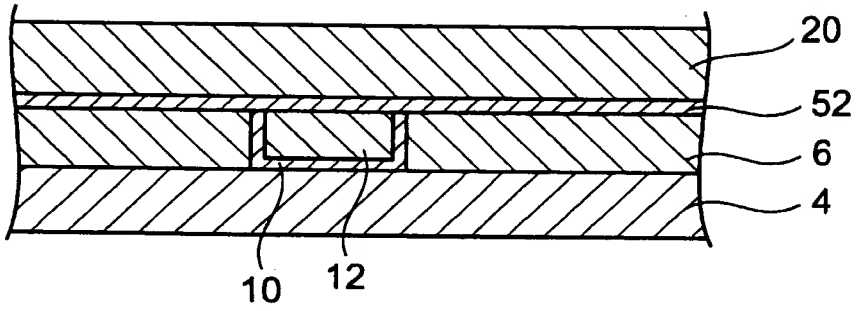
【図１】 Fig. 1



【図３】Fig. 3



【図４】Fig. 4



[NAME OF DOCUMENT] ABSTRACT OF THE DISCLOSURE

[ABSTRACT]

[PROBLEM] The present invention relates to an interlevel insulation in a semiconductor device whereby any aggregation is not caused in Cu formed by damascene.

[SOLVING MEANS] A multilayered Cu diffusion preventive insulating layer of not less than two layers is formed on a Cu interconnection by CVD. In this case, a first insulating film 16 of a first layer is formed at a low temperature of less than 300°C, and a second insulating film 18 of a second layer is formed at a high temperature within a range of 350°C to 450°C.

By this, any aggregation is not caused in Cu, and in addition such a function as being a protective layer upon applying an etching is brought out.

[DRAWINGS TO BE SELECTED] Fig. 1